

LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A programmable analog-to-digital converter (ADC) system comprising:
a quantizer assembly, configurable to provide at least one quantization stage, a given quantization stage converting an associated analog signal into an associated digital output signal; and

a configuration control that selects among a plurality of configurations and configures the ADC system according to the selected configuration, the quantizer assembly being configurable to provide a plurality of quantization stages arranged in series in a first configuration, and the quantizer assembly being configurable to provide a single quantization stage in a second configuration.

2. (Original) The system of claim 1, further comprising a switch fabric operative to selectively couple a plurality of components associated with the programmable ADC system in response to control input from the configuration control.

3. (Original) The system of claim 1, further comprising at least one configurable digital-to-analog converter (DAC).

4. (Currently amended) The system of claim-4 3, the at least one configurable DAC comprising a delta-sigma modulator.

5. (Original) The system of claim 1, further comprising a digital processor that processes the at least one associated digital output signal from the at least one quantization stage to determine at least one characteristic of the at least one associated analog signal.

6. (Original) The system of claim 5, the configuration control adaptively selecting among the plurality of configurations according to feedback from the digital processor.

7. (Original) The system of claim 1, the configuration control selecting among the plurality of configurations according to user input.

8. (Original) The system of claim 1, further comprising a programmable filter assembly, configurable to provide at least one noise shaping filter, a given noise shaping filter processing the analog signal associated with a respective quantization stage to shape quantization noise associated with the respective quantization stage.

9. (Original) The system of claim 8, the given noise shaping filter being operative to provide at least one low noise frequency band associated with the respective quantization stage.

10. (Original) The system of claim 9, the given noise shaping filter comprising at least one variable element being programmable by the configuration control to alter at least one respective shape of the at least one low noise frequency band.

11. (Original) The system of claim 9, the given noise filter having an associated sample and hold component, the sample and hold component being driven by a clock circuit to control a sample rate at which the associated analog signal is provided to the respective quantization stage, the sample rate being associated with at least one respective center frequency of the at least one low noise frequency band.

12. (Original) The system of claim 11, the clock circuit being controlled by the configuration control to alter the at least one respective center frequency of the at least one low noise frequency band.

13. (Original) The system of claim 11, the clock circuit comprising a digital frequency synthesizer.

14. (Original) A programmable analog-to-digital converter (ADC) system, comprising means for selecting a configuration from a plurality of configurations associated with the programmable ADC;

means for quantizing an analog input signal; and

means for configuring the ADC system according to the selected configuration, the means for configuring including means for configuring the means for quantizing to provide two associated quantization stages arranged in series and means for configuring the means for quantizing to provide one associated quantization stage.

15. (Original) The system of claim 14, the means for configuring comprising means for configuring the ADC system as a flash ADC.

16. (Original) The system of claim 14, the means for configuring comprising means for configuring the ADC system as a half-flash ADC.

17. (Original) The system of claim 14, the means for configuring comprising means for configuring the ADC system as a single-bit delta-sigma ADC.

18. (Original) The system of claim 14, the means for configuring comprising means for configuring the ADC system as a multi-bit delta-sigma ADC.

19. (Original) The system of claim 14, the means for configuring comprising means for configuring the ADC system as a cascaded delta-sigma ADC.

20. (Original) The system of claim 14, the means for configuring comprising means for configuring the ADC system as a hybrid ADC system comprising a flash ADC and a delta-sigma ADC.

21. (Original) The system of claim 14, the means for configuring comprising means for configuring the ADC system as a multi-range ADC system comprising a plurality of quantization stages in parallel.

22. (Original) The system of claim 21, the means for configuring comprising means for configuring the ADC system as a multiple amplitude range ADC system, such that the plurality of quantization stages have associated amplitude ranges, the means for configuring further comprising means for adaptively adjusting the associated amplitude ranges of the plurality of quantization stages according to a determined amplitude of the analog input signal.

23. (Original) The system of claim 21, the means for configuring comprising means for configuring the ADC system as a multiple frequency range ADC system, such that the plurality of quantization stages have associated frequency ranges, the means for configuring further comprising means for adaptively adjusting one of the associated frequency ranges and respective associated amplitude ranges of the plurality of quantization stages according to a determined frequency content of the analog input signal.

24. (Original) A method of configuring a programmable analog-to-digital converter (ADC) comprising:

selecting between at least a first configuration and a second configuration, the first configuration being characterized in that a quantizer assembly associated with the programmable ADC is configured into a single quantization stage and the second configuration being characterized in that the quantizer assembly is configured into a plurality of quantization stages, with at least two of the plurality of quantization stages being configured in series; and configuring the quantizer assembly according to the selected configuration.

25. (Original) The method of claim 24, further comprising configuring a programmable filter assembly according to the selected configuration to provide at least one noise shaper, a given noise shaper being operative to provide delta-sigma modulation of an analog input signal in combination an associated one of the plurality of quantization stages.

26. (Original) The method of claim 24, further comprising converting an analog signal into a digital signal using the selected ADC configuration.

27. (Original) The method of claim 26, further comprising analyzing the digital signal to determine at least one property of the analog signal.

28. (Original) The method of claim 27, further comprising selecting between the first configuration and the second configuration according to the determined at least one property of the analog signal.